AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1 – 11. Cancelled.

12. (Currently Amended) A method of communicating with a field programmable gate array (FPGA), comprising:

establishing an interface between a host computer and said FPGA;

~~communicating~~ transmitting configuration information over ~~a communication~~ said interface in a first transmission mode to configure the FPGA to function according to a programmed configuration; and

~~carrying out communications~~ transmitting operation information over ~~the~~ said ~~communication~~ interface in a second transmission mode ~~to the FPGA functioning according to the programmed configuration~~.

13. (Original) The method according to claim 12, wherein the programmed configuration comprises operation as a virtual device under test in an In-Circuit Emulation system.

14. (Original) The method according to claim 12, wherein the programmed configuration comprises operation as a virtual microcontroller in an In-Circuit Emulation system.

15. (Currently Amended) The method according to claim 12, wherein ~~the communication~~ said interface comprises an IEEE 1284 compliant interface.

16. (Currently Amended) A method of communicating with a field programmable gate array (FPGA), comprising:

~~a host computer~~ communicating over ~~a communication~~ an interface between a host computer and said FPGA to configure ~~the~~ said FPGA to act as a virtual microcontroller;

executing instructions ~~on a microcontroller device~~ in synchronization ~~with the~~ on a microcontroller device and said virtual microcontroller; and

~~the host computer communicating with~~ transmitting information between said host computer and ~~the~~ said FPGA using ~~the same communication~~ said interface ~~used to configure the FPGA~~.

17. (Currently Amended) The method according to claim 16, wherein ~~the communication~~ said interface comprises an IEEE 1284 compliant interface.

18. (Currently Amended) The method according to claim 16, wherein ~~the~~ said FPGA is further configured to incorporate ~~the communication~~ said interface.

19. (Original) A method of communication with a field programmable gate array (FPGA), comprising:

connecting a host computer to the FPGA using a communication interface;

programming a configuration into the FPGA, the configuration incorporating an implementation of the communication interface; and

carrying out non-programming communication between the host computer and the FPGA using the communication interface.

20. (Original) The method according to claim 19, wherein the communication interface comprises an IEEE 1284 compliant interface.

21. (Original) The method according to claim 19, wherein the configuration further incorporating a virtual microcontroller.

22. (Original) The method according to claim 21, wherein the virtual microcontroller executes instructions in synchronization with a microcontroller to carry out In-Circuit Emulation functions.

23. (Currently Amended) A method of communicating with an FPGA, comprising:

~~communicating~~ transmitting information over a parallel communication interface of an FPGA to configure the FPGA to act as a parallel port to receive data from a host computer system and to configure the FPGA to operate as a virtual microcontroller;

~~the parallel port of the FPGA~~ receiving data and communicating control information at said parallel port of said FPGA, the virtual microcontroller operating in lock step with a microcontroller under test; and

commanding the FPGA with instructions from the host computer system using the communication interface that configured the FPGA.

24. (Original) The method according to claim 23, wherein the parallel port comprises an IEEE 1284 compliant parallel port.

25. (Original) The method according to claim 23, wherein bidirectional IEEE 1284 compliant communication is carried out using extended parallel port (EPP) mode communication over the parallel port.

26. (Original) The method according to claim 23, further comprising conducting In-Circuit Emulation functions using the parallel port.